MPC Test Card Details
Jeff Andresen 7/2/2002

This document has design information for the MPC Test card to be fabricated by Metro Circuits quote number 0205297JB and Fermilab PRN 21819. The order is for 10 tested MPC Test cards to be delivered to Fermilab with a 2 week delivery time. This is a 6 layer design with 3 trace layers FR4 printed circuit board. The traces can be ½ oz. or 1 oz. copper with a 4 mil minimum width and a 4 mil minimum clearance. The finished board thickness should be .062" + or – what it takes to get the correct controlled impedance.

This is a controlled differential impedance design. The differential impedance is to be 75 ohms for the 4 mil differential pair side by side traces on the trace layers to the GND plane.

The 4 mil wire bond pads should have 150 micro inches of nickel with 7 to 10 micro inches of gold over the nickel for aluminum ultrasonic wedge bonding.

All vias should be covered with soldermask. A HASL finish should be on the solder pads.

The following is the board stackup with the Gerber file extension.

Layer 1, top trace layer, trace layer 1, 75 ohm differential impedance	*.TOP	----------
Layer 2, inner 1, partial split power plane,	*.IN1	----------
Layer 3, GND, GND plane, reference for controlled impedance	*.GND	----------
Layer 4, Power, partial split power plane	*.PWR	----------
Layer 5, inner 2, trace layer 2 & power, 75 ohm differential impedance	*.IN2	----------
Layer 6, BOT, trace layer 3, 75 ohm differential impedance	*.BOT	----------

There are the following additional files.

*.SST	Top silkscreen layer
*.TAP	Drill tape files
*.ASC	Netlist file from the schematic.
COMPS.TXT	Components on board
CONN.TXT	connections on board
*.DRD	Drill drawing Gerber file
*.DTS	Drill tape summary
*.LIS	post processing report including apertures
*.GTD	GERBTOOL design file.

Please contact me if there are any technical questions and deliver the PCBs to me.

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